## **ACKNOWLEDGEMENT RECEIPT**

Electronic Version 1.1

Stylesheet Version v1.1.1

Title of Invention

EFS ID:

JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING DELAYED CLOCK AND METHOD THEREOF

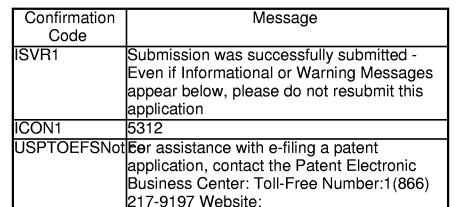
Submision Type: Utility Patent Filing

**Application Number:** 

10/711313

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Server Response:



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First Named Applicant: Jui-Hsing Tseng
Attorney Docket Number: MTKP0186USA

Timestamp: 2004-09-10 04:41:51 EDT

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